"Master mind" Marker

I.C. List

Gates		Counters		Decoders	
1x7414	1,2,3,4,5,6	7x7493	C1,2,3,4,5,6,7	2x7442	D1,D2
1x7402	7,8,9,10				
1x7408	11,12,13,14	Latches		J-K	
2x7486	15,16,17,18 21,22,23	2x74118	L1,L2	1x7473	F1,F2
1x7420	19,20				
1x7410	24,25,26	Multiplexers		Comparator	
		4x74153	M1,2,3,4	1x74L85	P1

Switches

S1-4	B.C.D. Thumb wheel
S5	PUSH TO MAKE
S6	S.P. TOGGLE
S7	S.P.C.O PUSH

Description

When switch S5 is depressed the latter stages of counters C1-4 perform a binary count of 0-5 or 0-6 depending on the position of switch S6. The gates 11-18 modify the normal binary count of 0-7. The first stages of counters C1-4 are used to produce a lower clock frequency output for control purposes.

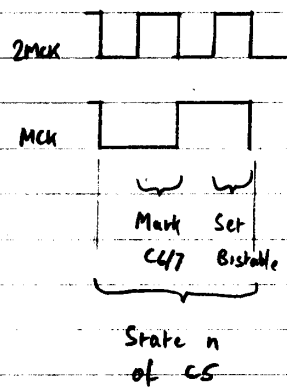
Switches S1-4 are used to produce 4 3 bit numbers which will be matched with those held in counters C1-4. Because the $\overline{8}$ output is not used positions 8 and 9 are identical with positions 0 and 1 respectively. Position 7 is not recognised and may be used for test purposes

Each switch and 'colour counter' (C1-4) are associated with one bi-stable each. When the colour switches have been set, the mark switch S7 is pushed in. This resets all of these bi-stables and clears the Mark counters C6-7. On the release of this switch the output of J-K F1 goes high and on the next negative going master clock pulse MCK, J-K F2 is set, $\overline{Q}_2$ going down releasing selection counter C5. This counter will count under the action of the master clock through binary counts 0-15. The outputs of this counter are modified to drive the select lines of multiplexers M1-4 and decoders D1,2. The action of the multiplexers is to direct the like bits of one switch and one counter to the comparator P1 and the output of the mark bistables to gate 10. The comparison sequence is as follows:-

Counter C5	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Compare Switch	1	2	3	4	2	1	4	3	3	4	1	2	4	3	2	1
to Counter	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4

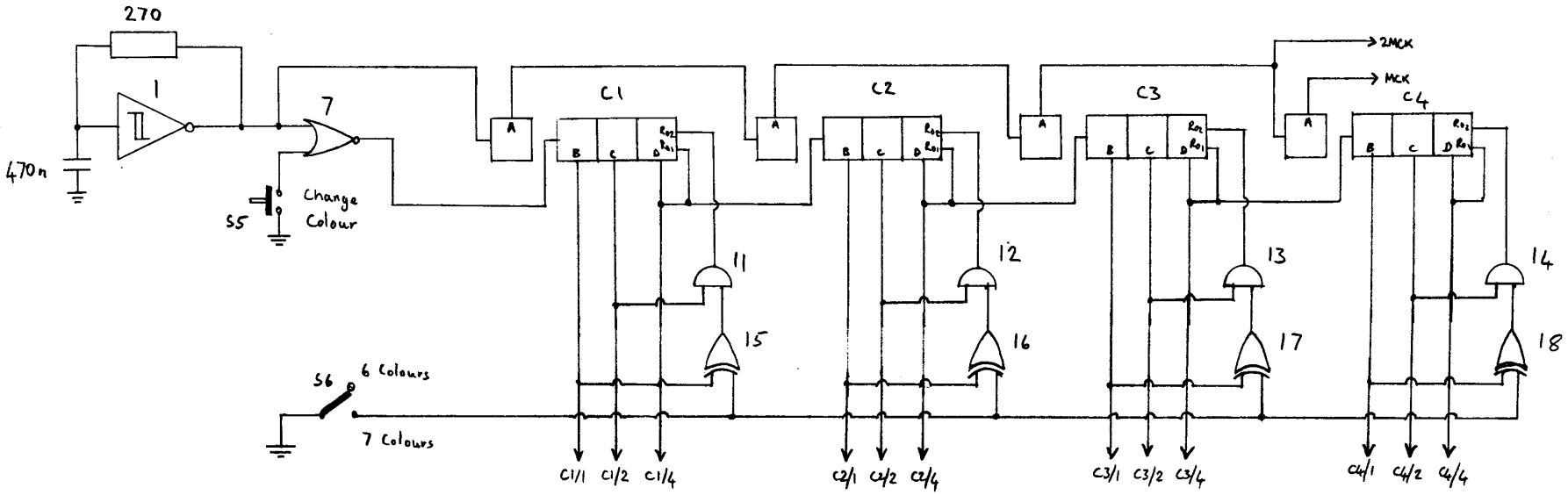
During C5 state 0, for example, counter C1 is compared with switch S1. If the numbers (colours) match counter C6 is incremented and mark bits CM1 and SM1 set via decoders D1,2. This setting process eliminates both S1 and C1 from comparison with other counters and switches during the cycle. It will be seen that the first four comparisons like numbered switch is compared with like numbered counter. Any parity noted here is equivalent to a 'block mark' ('right colour, right position'). Gate 8 recognises this first comparison cycle and directs marks to the 'block counter' C6. During the next three comparison cycles the switch and counter numbers are slipped. Any match during these periods are counted by the 'white counter' C7. At the end of the 16th master clock pulse all possible switch/counter combinations have been tried. The binary state 15 is recognised by gate 19 and used to reset J-K's F1, F2 and therefore terminating the marking process. Counters C6 - C7 retain the results of the comparison process.

Relation of marking pulses to counters to MCK, 2MCK and C5 state

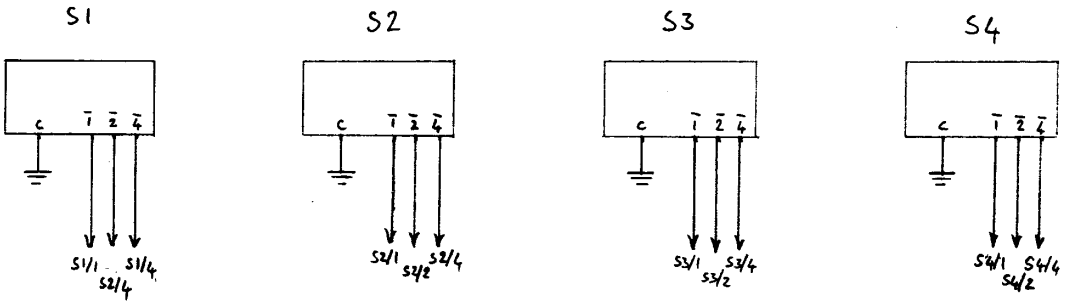


Notes

Input A3 to Comparator P1 is used to inhibit parity generation while J-K F2 is not set (i.e. marking not in progress). Cascade input A=B is also used for inhibiting parity if either of the marking bistables are set (previous match has been made with another switch/counter). Because a Low Power comparator is specified gate 23 is used as a buffer and performs no logical function.



SWITCH POSITION	0	1	2	3	4	5	6	7	8	9
COLOUR	BLACK	RED	YELLOW	GREEN	BLUE	WHITE	GREY		BLACK	RED



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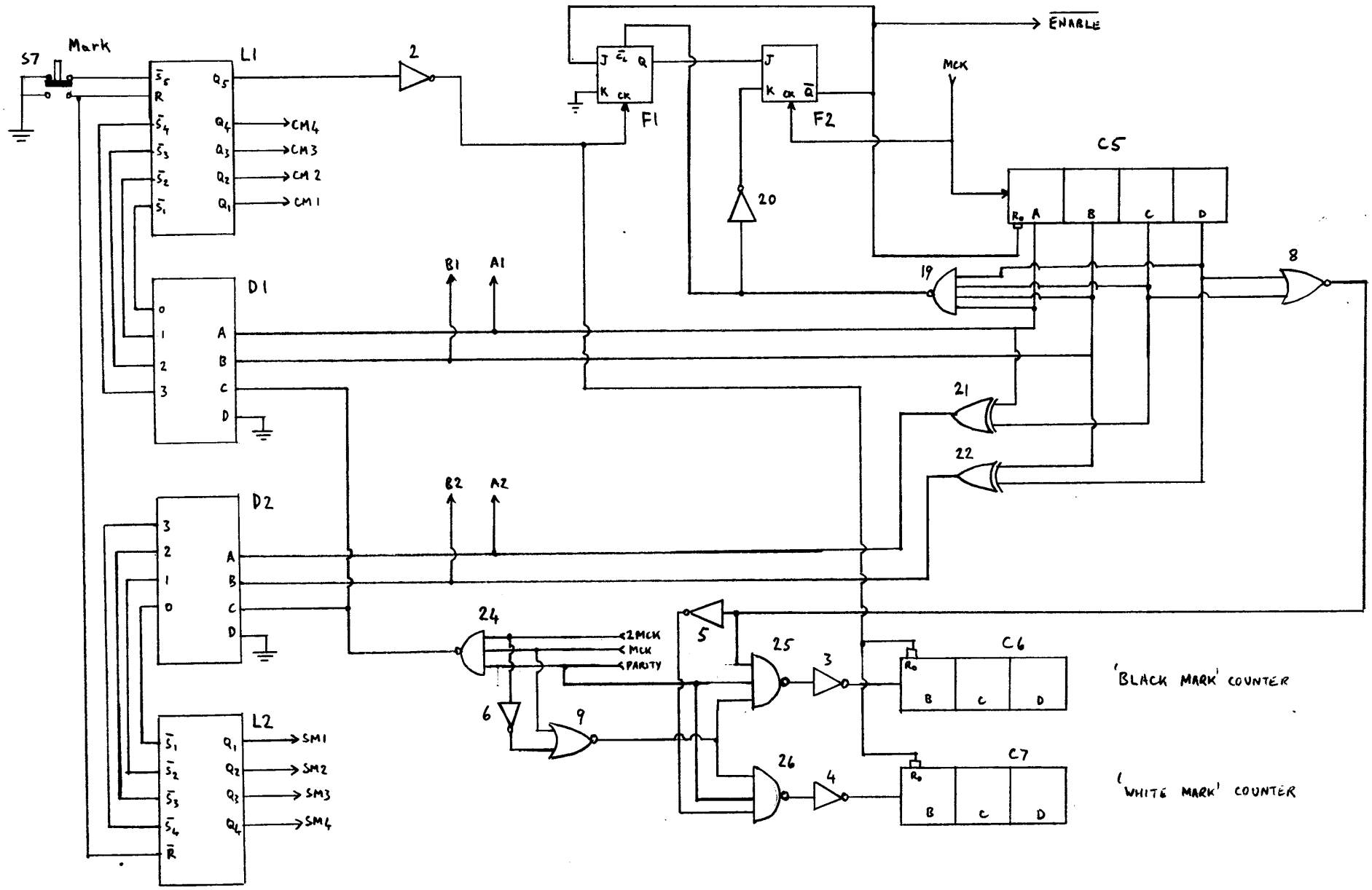

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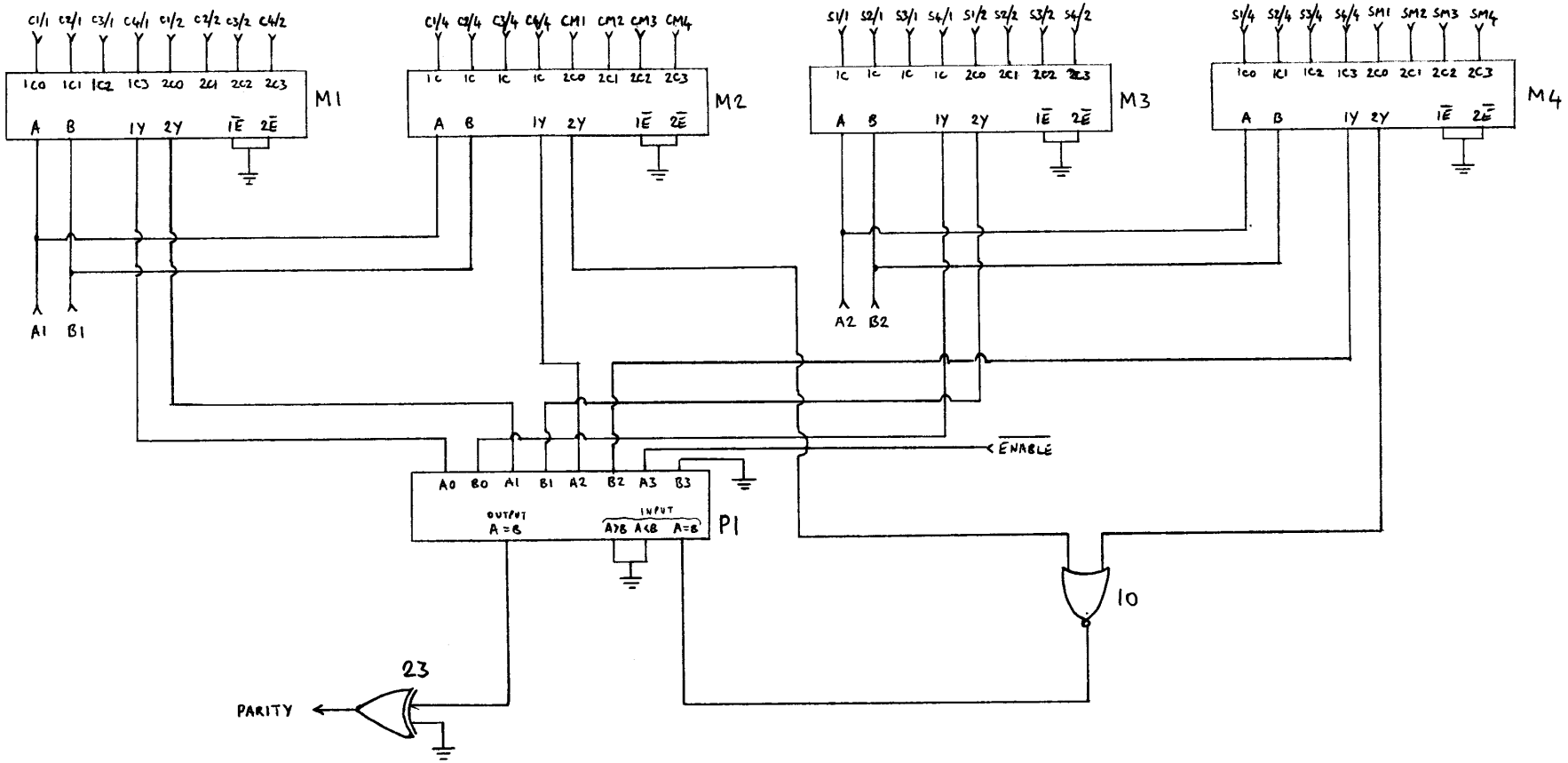

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